IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	BRETT D. LOWE ET AL.
Filed:	HEREWITH
For:	NON-OXIDIZING SPACER DENSIFICATION METHOD FOR MANUFACTURING SEDMICONDUCTOR DEVICES
Serial No.:	UNKNOWN
Group Art Unit:	UNKNOWN
Examiner:	UNKNOWN
Atty Docket No.:	ZILG518CON/ZILO:002C1

NUMBER: EV324157686US

I hereby certify that this paper or fee is being deposited with the United States Postal Service "EXPRESS MAIL POST OFFICE TO ADDRESSEE" service, postage prepaid, under 37 CFR 1.10 on the date indicated below and is address to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313.

Signature: Mary Jones Date: 9-22-03

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97, and 1.98, it is respectfully requested that this Information Disclosure Statement be entered and the document(s) listed on attached Form PTO-1449 be considered by the Examiner and made of record.

In accordance with 37 C.F.R §§ 1.97(g),(h), this Information Disclosure Statement is not to be construed as a representation that a search has been made, and is not to be construed to be an admission that the information cited is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b).

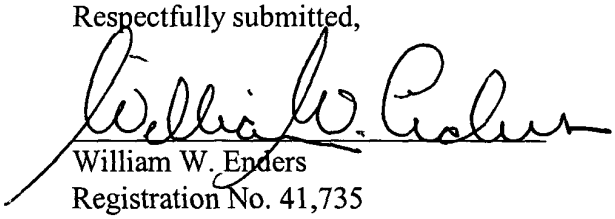
The present Information Disclosure Statement is being filed prior to the receipt of a

first Official Action reflecting an examination on the merits, and hence is believed to be timely filed in accordance with 37 C.F.R. § 1.97(b). No fees are believed to be due in connection with the filing of this Information Disclosure Statement, however, should any fees under 37 C.F.R. §§ 1.16 to 1.21 be deemed necessary for any reason relating to these materials, the Commissioner is hereby authorized to deduct said fees from Deposit Account No. 10-1205.

A copy of any listed document(s) that are required by 37 C.F.R. § 1.98(a)(2) are enclosed for the convenience of the Examiner.

Applicant respectfully requests that the listed document(s) be made of record in the present case.

Respectfully submitted,



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Form PTO-1449 (modified)	Atty. Docket No. ZILG518CON	Serial No. UNKNOWN
List of Patents and Publications for Applicant's **INFORMATION DISCLOSURE STATEMENT** (Use several sheets if necessary)	Applicant BRETT LOWE ET AL.	
	Filing Date: HEREWITH	Group: UNKNOWN

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Page 1	*N/A*	*See Pages 2-5*

U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date if App.
	A1	6,156,653	12/5/00	Smythe et al.			11/3/97
	A2	6,190,973 B1	2/20/01	Berg et al.			12/18/98
	A3	6,165,846	12/26/00	Carns et al.			3/2/99
	A4	5,089,432	2/18/92	Yoo			8/17/90
	A5	5,946,599	8/31/99	Lee et al.			7/24/97
	A6	5,710,454	1/20/98	Wu			4/29/96
	A7	5,422,311	6/6/95	Woo			5/2/94
	A8	5,541,131	7/30/96	Yoo et al.			2/1/91
	A9	5,986,312	11/16/99	Kuroda			9/3/97
	A10	5,130,266	7/14/92	Huang et al.			8/28/90
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	A18	6,146,970	11/14/00	Witek et al.			5/26/98

Foreign Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1						

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Exam. Init.	Ref. Des.	Citation
	C1	Krishna Seshan et al., "The Quality and Reliability of Intel's Quarter Micron Process," Intel Technology Journal Q3'98, pp. 1-11.
	C2	Y. G. Shen et al., "Qxygen-induced amorphous structure of tungsten thin films," Applied Physics letters, Volume 75, number 15, October 11, 1999, pp. 2211-2213.
	C3	Alain P. Blosse, "Improved Thermal Stability of CVD Wsi_x During Furnace Oxidation By A Rapid Thermal Anneal Pretreatment," Mat. Res. Soc. Symp. Proc. Vol. 525, 1998 Materials Research Society, pp. 371-377.
	C4	M. Doscher et al., "A study of WSi_2 Thin Films, Formed By The Reaction Of Tungsten With Solid Or Liquid Silicon, By Rapid Thermal Annealing," Thin Solid Films, 1994, pp. 251-258.
	C5	C.J. Backhouse et al., "WSi_x Thin Films For Resistors," Thin Solid Films, 1997, pp. 299-303.
	C6	A Fabricius et al., "Rapid Thermal Annealing Of Tungsten Silicide Films," Mat. Res. Soc. Symp. Proc. Vol. 402, 1996, Materials Research Society, pp. 625-630.
	C7	J. P. Gambino et al., "Thermal Stability of WSi_2 Polycide Structures For 1Gbit DRAMs," IEEE, 1998, pp. 259-261.
	C8	J.P. Gambino et al., "Reaction of Ti with WSi_2," American Institute of Physics, J. Appl. Phys. 82(12) December 15, 1997, pp. 6073-6077.
	C9	V. G. Glebovsky et al., "Properties of Tungsten Silicide Thin Films Obtained By Magnetron Sputtering Of Composite Cast Targets," Materials Research Society Symposium Proceedings, Vol. 402, November 27-30, 1995, 4 pgs.
	C10	Tohru Hara et al., "Properties of Sputtered Tungsten Silicide Films Deposited With Different Argon Pressures," Nuclear Instruments and Methods In Physics Research, B39, 1989, pp. 302-305.
	C11	H. Hayashida et al., "Dopant Redistribution In Dual Gate W-Polycide CMOS And Its Improvement By RTA," Semiconductor Device Engineering Laboratory, Integrated Circuit Division, Toshiba Corporation, 1989, 2 pgs.
	C12	Hoi Chung et al., "Effects Of The Phosphorus Doping Level And Excess Silicon On The Oxidation Of Tungsten Polycide," Journal of the Korean Physical Society, Vol. 29, No. 5, October 1996, pp. 658-663.
	C13	Masahiro Itoh et al., "Observation Of Microstructure At The Polycrystalline Silicon And Tungsten Silicide Interface," Applied Surface Science, 56-58, 1992, pp. 540-544.

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	C15	Takamaro Kikkawa et al., "0.35μm Technologies In Japan," ULSI Device Development Laboratories, Materials Research Society, Mat. Res. Soc. Symp. Proc. Vol. 402, 1996, pgs. 199-208.
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	C19	F. Mohammadi et al., "Properties Of Sputtered Tungsten Silicide For MOS Integrated Circuit Applications," J. Electrochem, Soc. Solid-State Science and Technology, February 1980, pp. 450-454.
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	C22	Krishna Shenai et al., "Structural And Electrical Properties Of Furnace And Rapid Thermally Annealed LPCVD WSi_2 Films On Single-Crystal, Polycrystalline, And Amorphous Silicon Substrates," IEEE Transactions On Electron Devices, Vol. 39, No. 1, January 1992, pp. 193-199.
	C23	M.P. Siegal et al., "The Formation Of Thin-Film Tungsten Silicide Annealed In Ultrahigh Vacuum," America Institute of Physics, J. Appl. Phys. 66(12), December 1989, pp. 6073-6076.
	C24	A.K. Sinha, "Refractory Metal Silicides For VLSI Applications," American Vacuum Society, J. Vac. Sci. Technol., 19(3), September-October 1981, pp. 778-785.
	C25	John Smythe et al., "A Structural And Bonding Perspective Of The Anomalous Oxidation Of Tungsten Polycide," MSE510 Term Project Paper, December 9, 2000, 17 pgs.
	C26	H. Tsutsui et al., "Suppression Of Partial Corrosion Of Sputtered Wsix Gate In HF Solution," Electrochemical Society Proceedings, Vol. 96-2, 1996, pp. 226-232.

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	C28	Chapter 11: "Refractory Metals and Their Silicides in VLSI Fabrication," Silicon Processing for the VLSI Era, 1986, pp. 384-406.
	C29	George E. Georgiou, Chapter 2: "Silicides and Contacts for ULSI," Multilevel Metallization for Integrated Circuits, pp. 32-91.
	C30	S. M. Sze, "p-n Junction Diode," Physics of Semiconductor Devices, Second Edition, Ch. 2, 1981, pp. 63-132.
	C31	J.C. Dupuy et al., "Dopant Redistribution During The Formation Of Tungsten Disilicide By Rapid Thermal Processing," Materials Science and Engineering, B22 (1994), pp. 168-171.
	C32	S. L. Zhang et al., "The Influence of Substrate Doping On Silicide Formation With Tungsten Deposited From Tungsten Hexafluoride," Mat. Res. Soc. Symp. Proc. Vol. 260, Materials Research Society, 1992, pp. 411-416.
	C33	C. B. Cooper III et al., "Dopant Redistribution in Silicides: Materials and Process Issues," J. Vac. Sci. Technol. B2 (4), Oct.-Dec. 1984, 1984 American Vacuum Society, pp. 718-722.
	C34	Tae-Hyung Kim et al., "LPCVD WSi_x/poly-Si W-polycide, The Properties of W-Polycide On Thickness Changes of the WSi_x/poly-Si Films Deposited By LPCVD," Trans. KIEE, Vol. 41, No. 10, Oct. 1992, pp. 1172-1179.
	C35	S. Nygren et al., "Dopant Redistribution From Ion Implanted WSi_2 On Poly-Si,"Elsevier Science Publishers B.V. (North-Holland), 1988, pp.419-422.
	C36	F. C. Shone et al., "Modeling Dopant Redistribution in $SiO_2/WSi_2/Si$ Structure," 536-IEDM 86, December 1986, 4 pgs.
	C37	J. Torres et al., "Phosphorus Redistribution in a WSi_2/Poly-Si Gate Structure During Furnace Annealing," March 1987, 4 pgs.
	C38	Chongmu Lee et al., "Effects of the Annealing Treatment on the Oxidation Behaviors of Tungsten Silicide," Korean Applied Physics (Korean Physical Society) Vol. 3, No. 2, May 1990, pp. 235-240.
	C39	Hoi Hwan Chung et al., "poly-Si/SiO_2/Si - Study on Formation of W-Silicide in the Doped-Phosphorus poly-Si/SiO_2/Si-Substrate," Dept. of Electronic Eng., Kyunghee Univ., Div. of Elec. & Infor. Technology, KIST, 1996, pp. 126-134.

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Exam. Init.	Ref. Des.	Citation
	C40	Co-pending United States Patent Application Serial No. 09/918,364 filed July 30, 2001 (ZILG:518/ZILO:002) which is relied upon by the present application for an earlier effective filing date under 35 U.S.C. Section 120

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